Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for determining the integrity of a memory under a plurality of operating environments comprising:

setting a plurality of operating environments for a condition to be tested;

testing the memory under the plurality of operating environments, respectively;

recording a result of the testing step for each of the plurality of operating environments; and

comparing the recorded results for the plurality of operating environments.

[c2] 2.The method of claim 1 wherein the testing step further comprises:

performing a built-in self test (BIST) on the memory under each operating environment.

[c3] 3.The method of claim 2 further comprising:

marking a status record memory according to the BIST, wherein the status record memory corresponds to the memory; and

recording the content of the status record memory for each operating environment.

[c4] 4.The method in claim 1 wherein the condition to be tested is a variance in supply voltage.

[c5] 5.The method in claim 1 wherein the condition to be tested is a variance in temperature.

[c6] 6.The method of claim 1 wherein the testing step further comprises:
detecting information concerning defects in the memory.

[c7] 7.The method in claim 6 wherein the recording step further comprises:
recording the number of defects detected in the memory.

[c8] 8.The method in claim 7 wherein the comparing step further comprises:
determining if the numbers of defects corresponding to the plurality of operating environments equal to one another.

[c9] 9.The method in claim 6 wherein the recording step further comprises:
recording the position of each defect detected in the memory.

[c10] 10.The method in claim 9 wherein the comparing step further comprises:

determining if the positions of defects corresponding to the plurality of operating environments are the same as one another.

[c11] 11. A method for determining the integrity of a memory, comprising:
testing the memory under a first operating environment;
recording a first result of the testing step under the first operating environment;
testing the memory under a second operating environment;
recording a second result of the testing step under the second operating environment; and
comparing the first result with the second result.

[c12] 12.The method of claim 11 wherein the testing steps further comprises:
performing a built-in self test (BIST) on the memory.

[c13] 13.The method of claim 12 further comprising:
marking a status record memory according to the BIST, wherein the status record memory corresponds to the memory; and
recording the content of the status record memory for the current operating environment.

[c14] 14.The method in claim 11 wherein the difference of the

first and the second operating environment lies in supply voltage.

[c15] 15.The method in claim 11 wherein the difference of the first and the second operating environment lies in temperature.